QMP03M60
Intelligent Power Module

Features

- Integrated 6 fast recovery power MOSFETs (600V/3A)
- Integrated high voltage gate drive circuit (HVIC)
- Compatible with 3.3V & 5V input signal, effective at high level
- Insulation class 1500Vrms / min
- Integrated bootstrap functionality
- High reliability and thermal stability, good parameter consistency
- Integrated temperature output

Applications

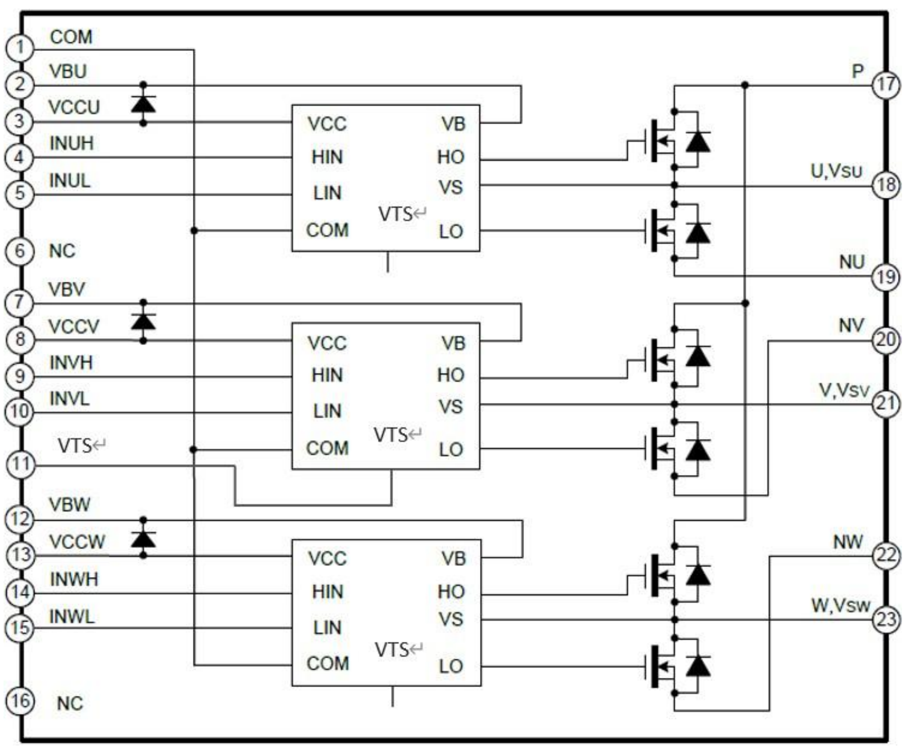
- Frequency conversion fans
- Cooker hood
- Air conditioning compressor
- Dish washer
- Air cleaner

Product Name	Marking	Package Type
QMP03M60TA	QMP03M60TA	DIP-23H
QMP03M60TD	QMP03M60TD	SOP-23H

DIP-23H

SOP-23H

Internal Electrical Schematic



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC link supply voltage of P-N	V_{PN}	600	V
Single MOSFET output current， T_C=25℃	I_{D25}	3.0	A
Single MOSFET output current， T_C=80℃	I_{D80}	2.5	
Single MOSFET peak output current T_C=25℃, pulse width <100μs	I_{DP}	5	A
Power dissipation per MOSFET, T_C=25℃	P_D	13.9	W
Module supply voltage	V_{CC}	25	V
High side floating supply voltage (V_B reference to V_S)	V_{BS}	20	V
Input voltage	V_{IN}	-0.3~VCC+0.3	V
Operating junction temperature	T_J	-55 to 150	℃
Operating case temperature, TJ≤150°C	T_C	-55 to 150	
Storage temperature range	T_{STG}	-55 to 150	℃
Single MOSFET thermal resistance, junction-case	$R_{θJC}$	9	℃/W
Isolation test voltage (1min, RMS, f = 60Hz)	V_{ISO}	1500	Vrms
Bootstrap diode forward current，T_C=25℃	I_F	1	A
Bootstrap diode peak forward current，T_C=25℃， pulse width =1ms	I_{FP}	3	A

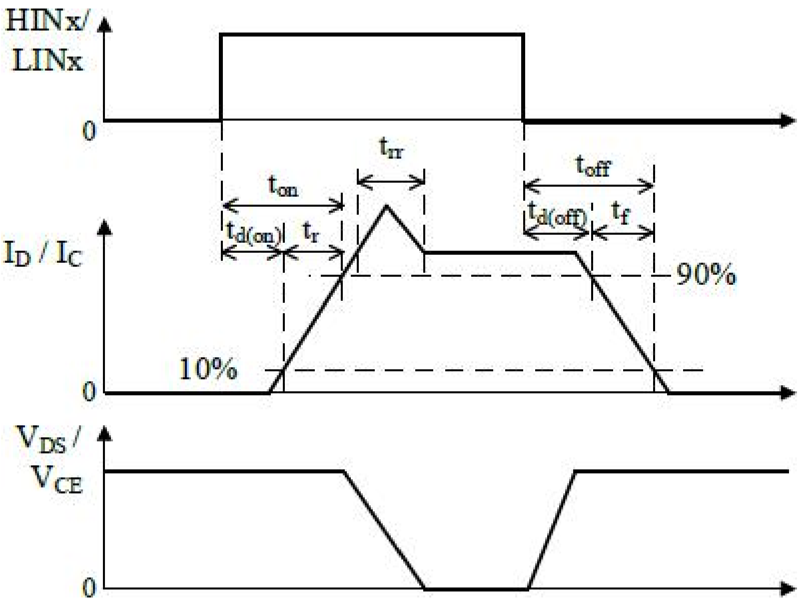
Recommended Operation Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	-	300	400	V
Low side supply voltage	V_{CC}	13.5	15	16.5	V
High side floating supply voltage	V_{BS}	13.5	15	16.5	V
Logic "1" input voltage (LIN, HIN)	$V_{IN(ON)}$	2.5	-	-	V
Logic "0" input voltage (LIN, HIN)	$V_{IN(OFF)}$	-	-	0.8	V
External deadtime between HIN and LIN	Tdead	-	540	-	ns
PWM switching frequency，T_J≤150ºC	fPWM	-	16	-	KHz

Electrical Characteristics（unless otherwise noted，T_j=25℃，V_{CC}=V_{BS}=15V）

Inverter Section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Drain-Source blocking voltage	B_{VDSS}	V_{IN}=0V，I_D=250uA	600	-	-	V
Drain-Source leakage current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	-	-	1	uA
Drain-Source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1.5A	-	2.8	3.4	Ω
Diode forward voltage	V_{SD}	V_{SG}=0V, Is=1.5A	-	-	1.4	V
Switching time	t_{ON}	V_{PN}=300V, V_{CC}=V_{BS}=15V I_D=0.5A, V_{IN}=0V~5V, Inductive load	-	820	-	ns
	t_{OFF}		-	500	-	ns
	t_{rr}		-	75	-	ns
	E_{ON}		-	75	-	uJ
	E_{OFF}		-	8	-	uJ



Switching Time Definition

Control Section

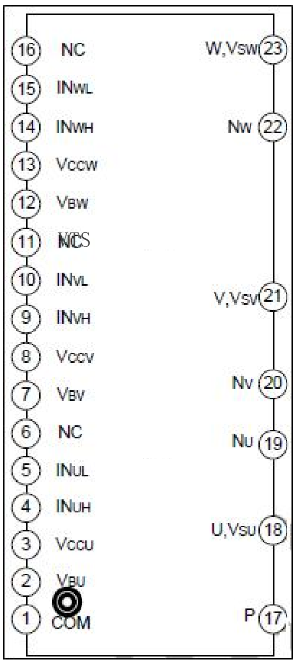
Parameter	Symb ol	Condition	Value			Uni t
Quiescent VCC supply current	I_{QCC}	VBIAS (V_{CC}, V_{BS}) =15V TA = 25°C	-	160	-	μA
Quiescent VB supply current	I_{QBS}		-	70	120	

Temperature output voltage	VTS	V phase HVIC temperature @25℃		600	790	980	mV
		V phase HVIC temperature @100℃		2.0	2.25	2.5	V
Low side undervoltage protection	UV_{CCR}	Reset level		8	8.9	9.8	V
High side undervoltage protection	UV_{BSR}	Reset level		8	8.9	9.8	V
Logic "1" input voltage (LIN, HIN)	V_{IH}	Logic high level	Between input and COM	2.5	-	-	V
Logic "0" input voltage (LIN, HIN)	V_{IL}	Logic low level		-	-	0.8	V
Input bias current for LIN, HIN	I_{IH}	VIN=5V	Between input and COM	-	6	15	μA
	I_{IL}	VIN=0V		-	-	1	

Bootstrap diode section

Parameter	Symbol	condition	Value			Unit
			Min.	Typ.	Max.	
Forward voltage	V_F	I_F=1A@ T_j=25℃	-	1.35	1.8	V
		I_F=1A@ T_j=125℃	-	-	1.6	
Reverse recovery time	t_{rr}	I_F=1A, V_R=30V, di_F/dt=-200A/μs	-	-	45	ns

Pin Assignment



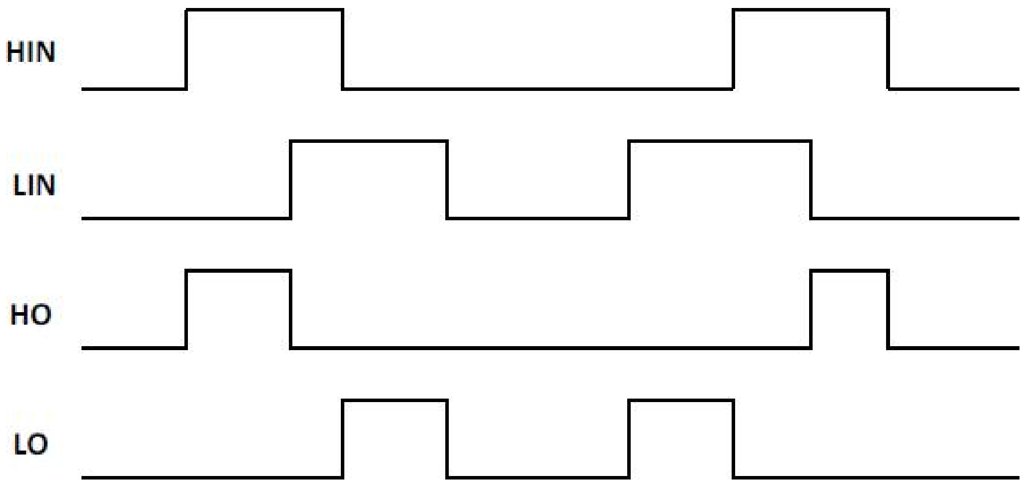
Pin Description

Pin Number	Pin name	I/O	Pin Description
1	COM	I/O	Module common ground
2	V_{BU}	I/O	U-phase high side floating IC supply voltage
3	V_{CCU}	I/O	U-phase low side driver supply voltage
4	I_{NUH}	I	U-phase high side gate driver input
5	I_{NUL}	I	U-phase low side gate driver input
6	NC	I/O	No Connection
7	V_{BV}	I/O	V-phase high side floating IC supply voltage
8	V_{CCV}	I/O	V-phase low side driver supply voltage
9	I_{NVH}	I	V-phase high side gate driver input
10	I_{NVL}	I	V-phase low side gate driver input
11	VTS	O	Temperature sensing output signal
12	V_{BW}	I/O	W-phase high side floating IC supply voltage
13	V_{CCW}	I/O	W-phase low side driver supply voltage
14	I_{NWH}	I	W-phase high side gate driver input
15	I_{NWL}	I	W-phase low side gate driver input
16	NC	I/O	No Connection
17	P	I/O	Positive bus input voltage
18	U,V_{SU}	O	Motor U-phase output and U-phase high side drive bias voltage ground
19	NU	I/O	U-phase low side source
20	NV	I/O	V-phase low side source
21	V,V_{SV}	O	Motor V-phase output and V-phase high side drive bias voltage ground
22	NW	I/O	W-phase low side source
23	W,V_{SW}	O	Motor W-phase output and W-phase high side drive bias voltage ground

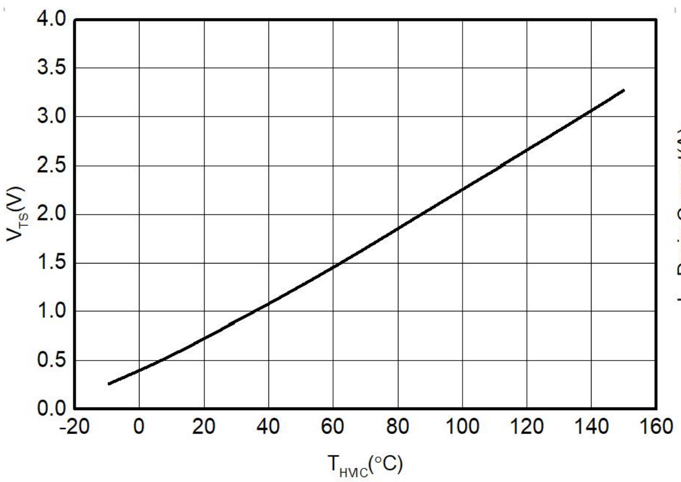
Function description

Input-output table

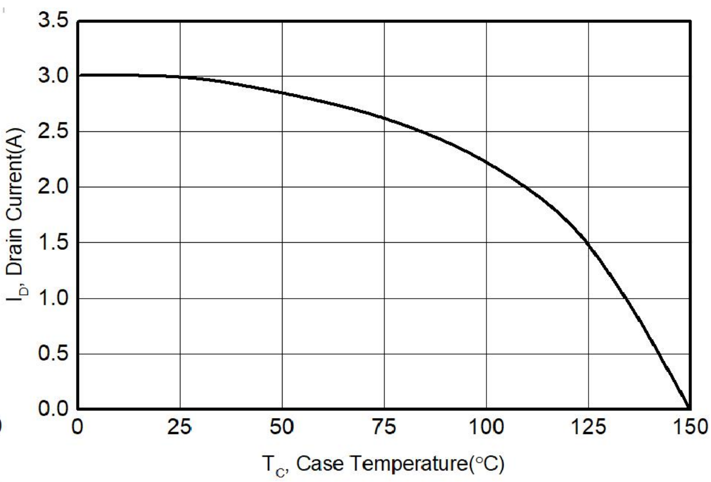
INH	INL	OUTPUT	REMARK
0	0	Z	The high and low sides of the bridge arm are closed
0	1	0	The low side of the bridge arm is opened
1	0	VDC	The high side of the bridge arm is opened
1	1	Forbid	Bridge arm punch through
Open	Open	Z	The high and low sides of the bridge arm are closed



Control sequence diagram

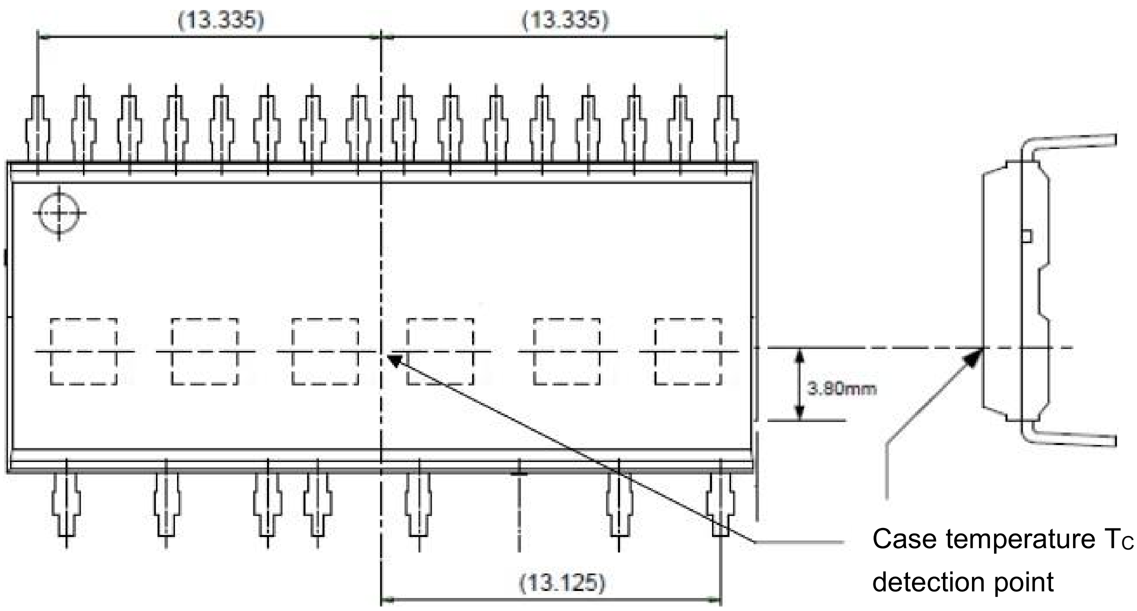


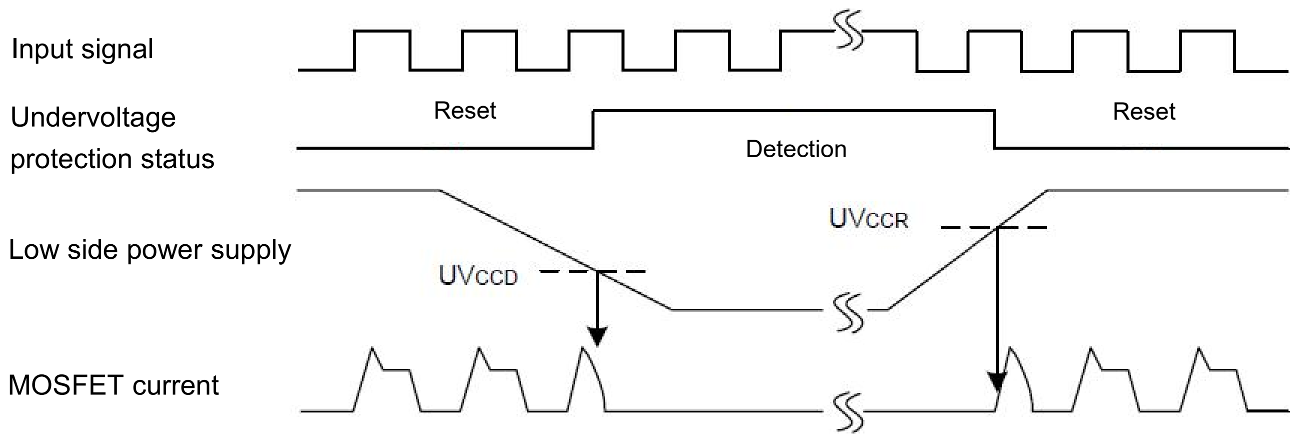
Temperature Profile of V_{TS}(Typical)



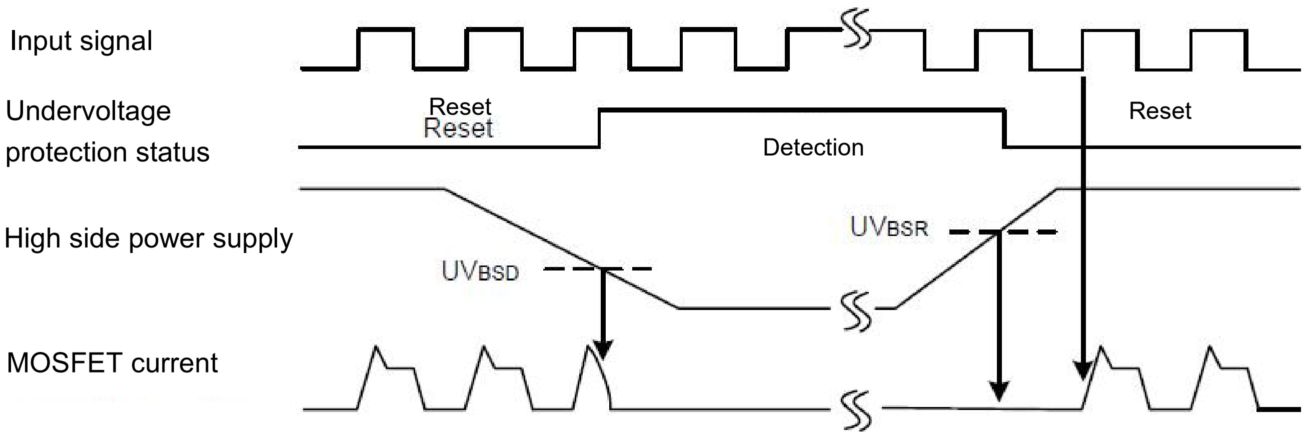
I_D Drain Current vs. Case Temperature

Case temperature Tc detection



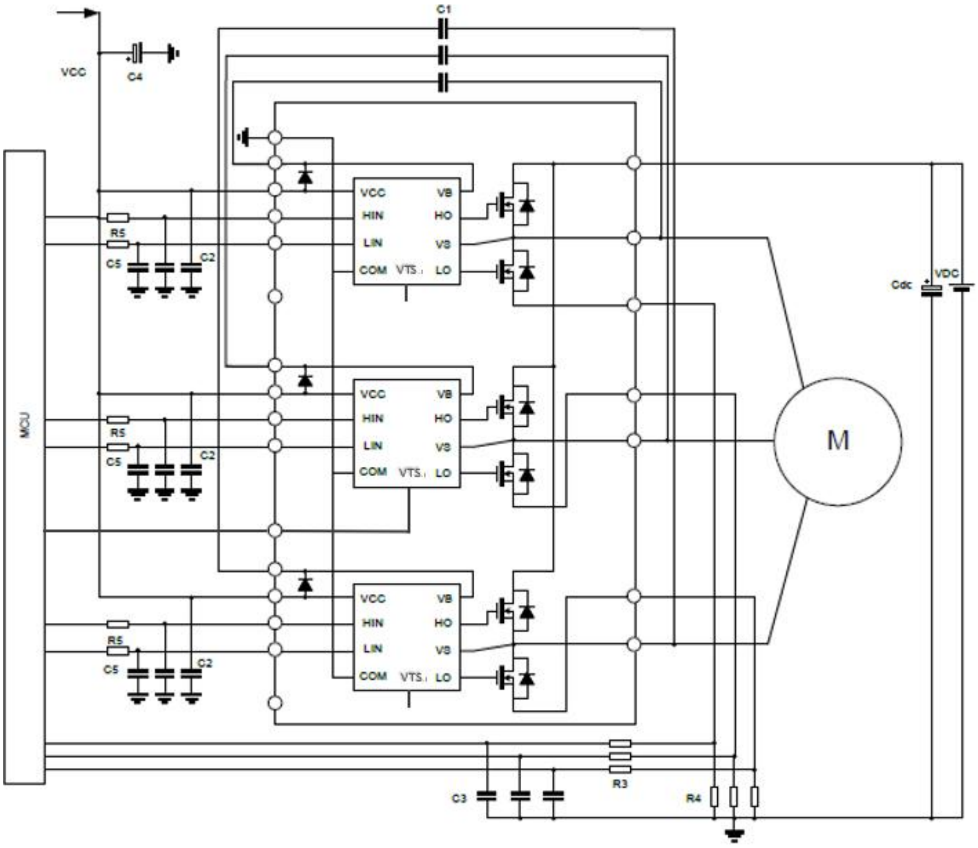


Undervoltage protection（Low side）



Undervoltage protection（High side）

Typical Application Schematic:



Remark:

(1) The wiring of each input pin shall be as short as possible, otherwise it may cause mis operation； in addition, RC filter can be used to reduce input signal noise.

(2) All external capacitors should be located close to IPM.

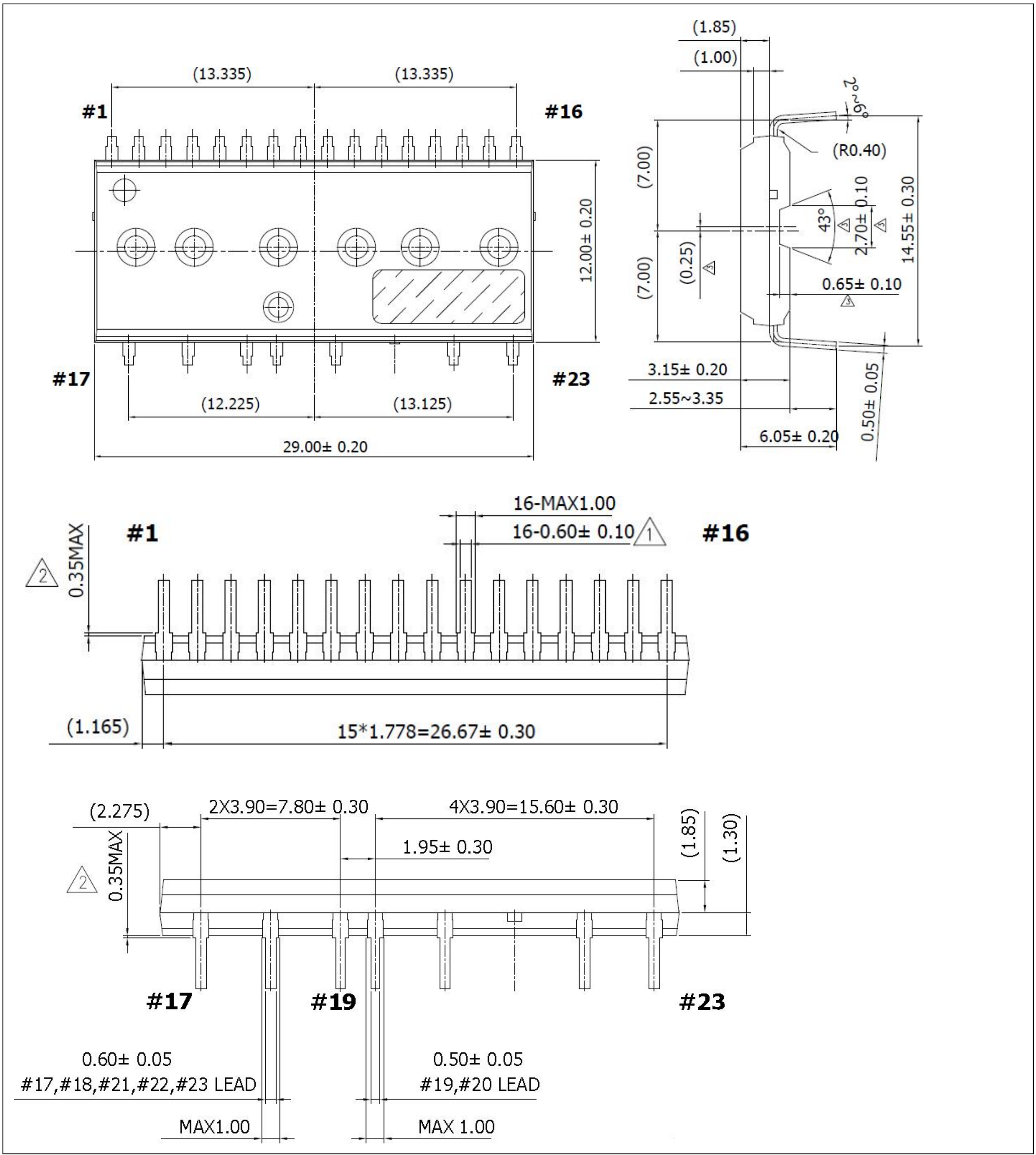
(3) In order to prevent surge damage, in addition to filter capacitance between PN, it is recommended to add a high-frequency non inductive smoothing capacitance, and the connection of capacitance should be as short as possible.

(4) The filter capacitance at the input of VCC power supply is recommended to be at least 7 times of bootstrap capacitance C1.

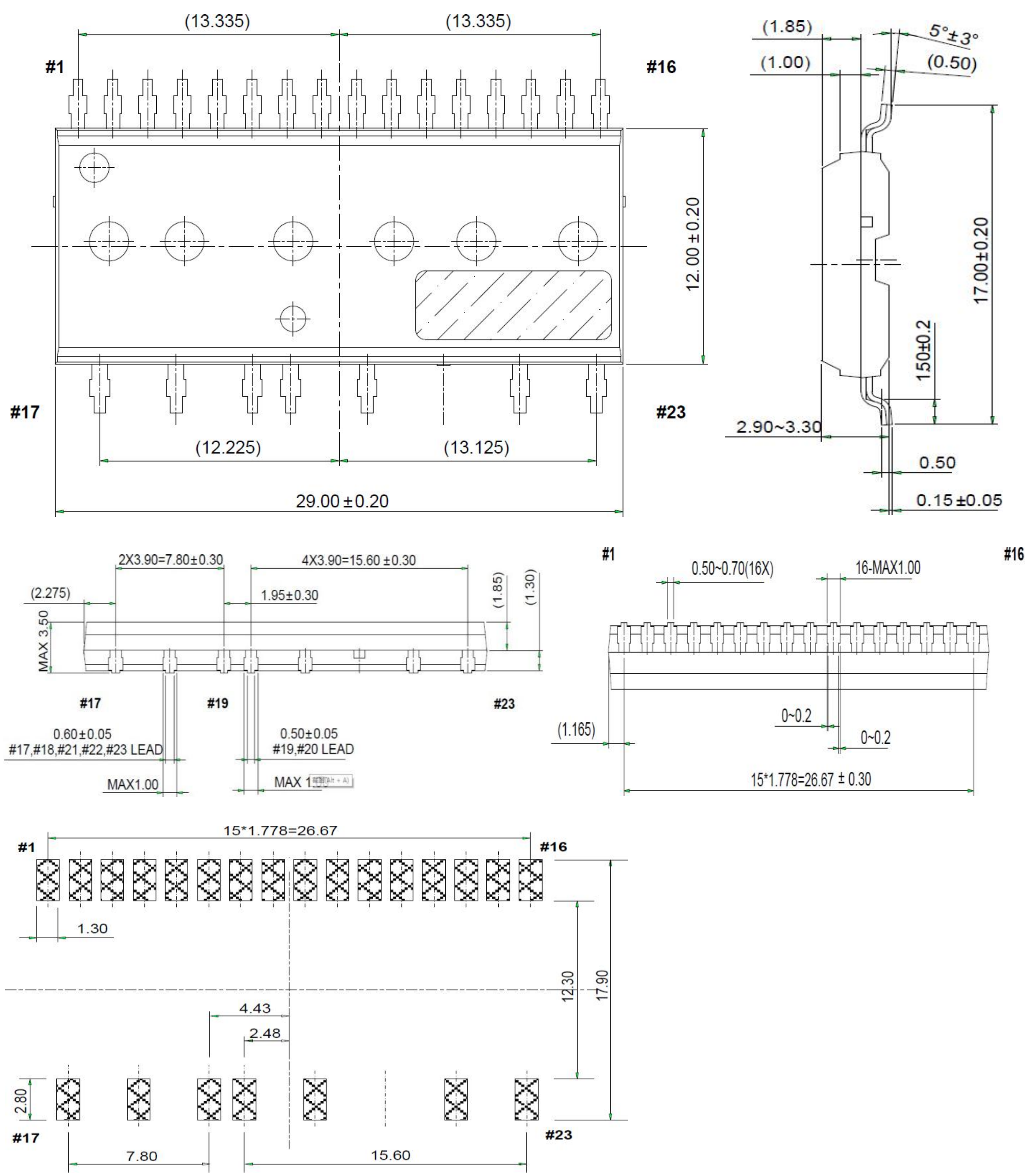
(5) The bootstrap capacitor C1 is suggested to adopt a capacitor with high frequency characteristics to absorb high frequency ripple current, and its capacitance value is suggested to be greater than 2.2uf.

(6) The connection between current limiting resistor R4 and IPM shall be as short as possible to prevent the large surge voltage generated by the connection inductance from damaging IPM.

Package Outline DIP23



Package Outline SOP23



Disclaimer:

Operating conditions may differ from simulation assumptions in several aspects like level of DC-link voltage, applied gate-voltage and gate-resistor, case and junction temperatures as well as the power circuit stray-inductance. Therefore, deviations of parameters and assumptions used for the simulation and the real application may exist.

For these reasons we cannot take any responsibility or liability for the exactness or validity of the form's results. The form cannot replace a detailed reflection of the customers application with all of its operating conditions.

Accurate results depend on huge data，so with the measured data is increasing, we should be updated in real time and send it to the corresponding engineer so that he can know it in real time.